

MB Board Information:

1. DA6001W000, PCB 29L LA-G07EP REV0 MB 3(KBLU\_26)

2. DA6001W000, PCB 29L LA-G07EP REV0 MB 3(KBLU\_26)

3. DA6001W000, PCB 29L LA-G07EP REV0 MB 3(KBLU\_26)

4. DA6001W000, PCB 29L LA-G07EP REV0 MB 3(KBLU\_26)

5. DA6001W000, PCB 29L LA-G07EP REV0 MB 3(KBLU\_26)

6. DA6001W000, PCB 29L LA-G07EP REV0 MB 3(KBLU\_26)

7. DA6001W000, PCB 29L LA-G07EP REV0 MB 3(KBLU\_26)

8. DA6001W000, PCB 29L LA-G07EP REV0 MB 3(KBLU\_26)

Sub Board Information:(EPK52)

01.DA6001W000, PCB 29L LA-G07EP REV0 IOB(4350M32L01)

02.DA6001W000, PCB 29L LA-G07EP REV0 HDD(4350M32L01)

03.DA6001W000, PCB 29L LA-G07EP REV0 TOUCH(4350M32L01)

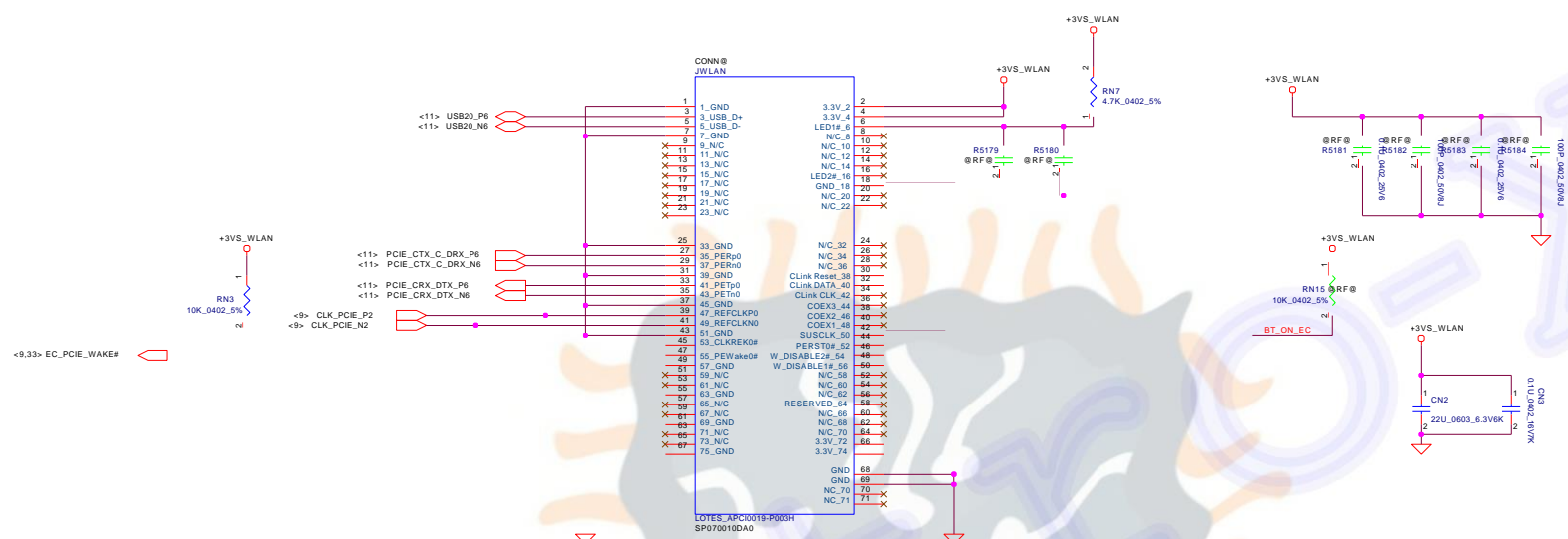
04.DA6001W000, PCB 29L LA-G07EP REV0 SSD(4350M32L01)

05.DA6001W000, PCB 29L LA-G07EP REV0 GMMCB

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2017/08/24	Deciphered Date	2018/08/24	Block Diagrams	
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				Date	Monday, January 08, 2018
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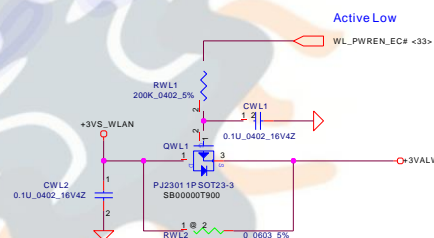
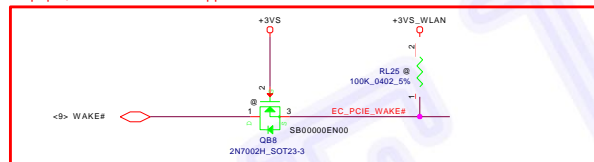


<6,7,9,10,11,13,17,18,27,28,29,31,32,33,36,39,40,52> +3VS  
<7,13,29,33,34,35,40,48,49,50,51> +3VALW

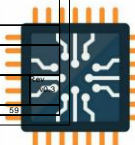


## NGFF and WLAN

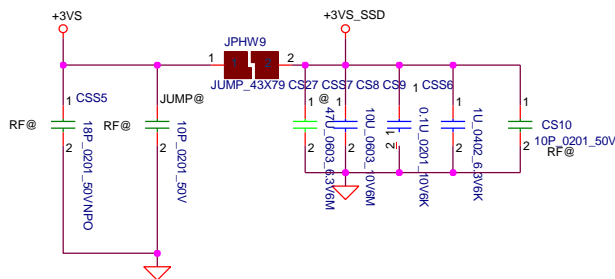
Unpop QB8 and RL25 for not support OBF



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Date: Friday, January 05, 2018				Sheet 30 of 33







<6,7,9,10,11,13,17,18,27,28,29,30,32,33,36,39,40,52>

+3VS

+3VS

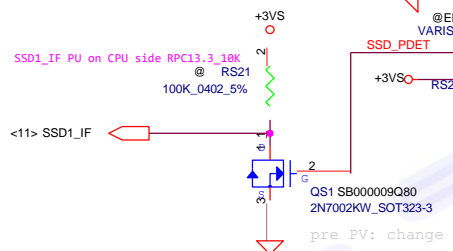
Figure 12-1. PCI Express® Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details	PCIe® Controller #1				PCIe® Controller #2				PCIe® Controller #3			
Flex I/O Lane #	5	6	7	8	9	10	11	12	13	14	15	16
PCIe® Lane #	1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1			RP 5				RP 9			
	1x4 LR	RP 1			RP 5				RP 9			
	2x2	RP 1	RP 3	RP 4	RP 5				RP 9			
	1x2+2x1	RP 1	RP 3	RP 4	RP 5				RP 9			
	2x1+1x2	RP 4	RP 3	RP 1	RP 5				RP 9			
Premium-U	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11
	1x4	RP 1			RP 5				RP 9			
	1x4 LR	RP 1			RP 5				RP 9			
	2x2	RP 1	RP 3	RP 4	RP 5				RP 9			
	1x2+2x1	RP 1	RP 3	RP 4	RP 5				RP 9			

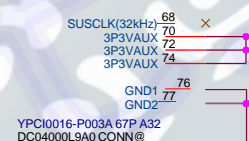
<SSD>

<11> PCIE\_CRX\_DTX\_N11  
<11> PCIE\_CRX\_DTX\_P11  
<11> PCIE\_CTX\_C\_DRX\_N11  
<11> PCIE\_CTX\_C\_DRX\_P11  
<11> PCIE\_CRX\_DTX\_P12  
<11> PCIE\_CRX\_DTX\_N12  
<11> PCIE\_CTX\_C\_DRX\_N12  
<11> PCIE\_CTX\_C\_DRX\_P12

<9> CLK\_PCIE\_N4  
<9> CLK\_PCIE\_P4



pre PV: change to 10K for redriver detect pin voltage level

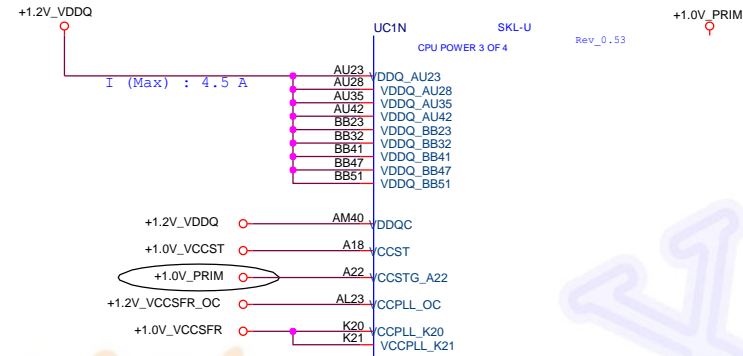


39	GND	PCIM/Mm_D09000NU90_MZVLW1T0HMLH-000H1_F73H1Q_09H	40	GND	Return Current Path
41	PET0	PCIe TX	42	N/C	
43	PET1	PCIe TX	44	N/C	
45	GND	Return current path	46	N/C	
47	PER0	PCIe Rx	48	N/C	
49	PER1	PCIe Rx	50	PERST#	
51	GND	Return current path	52	CLKREQ#	



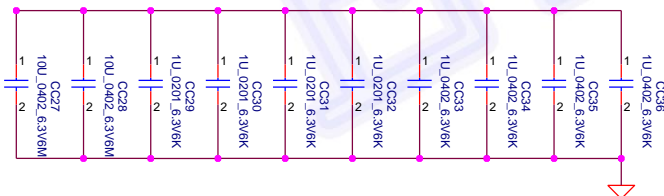
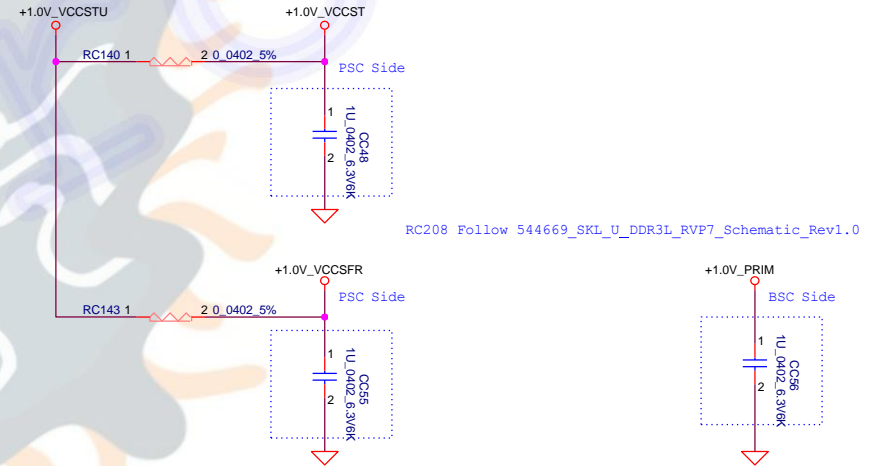
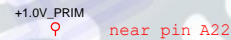
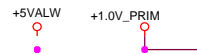


+1.0V\_PRIM TO +1.0V\_VCCSTU

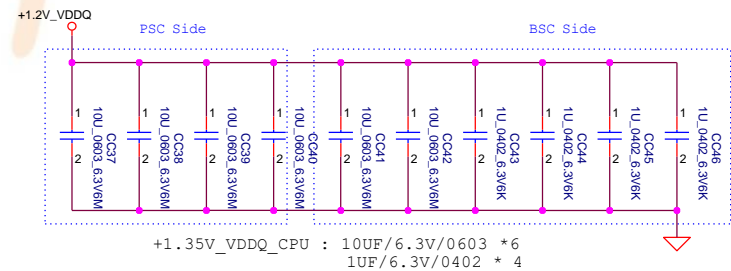
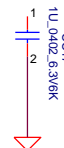


<Cocoa\_1113>  
Per  
543977 SKL PDDG Rev0\_91,  
change CC95 value from  
1000pf to 10pf for meet  
<= 65us timing for  
+1.0V\_VCCSTU power rail.

+1.0V\_PRIM TO +1.0VS\_VCCSTG / +1.0VS\_VCCIO

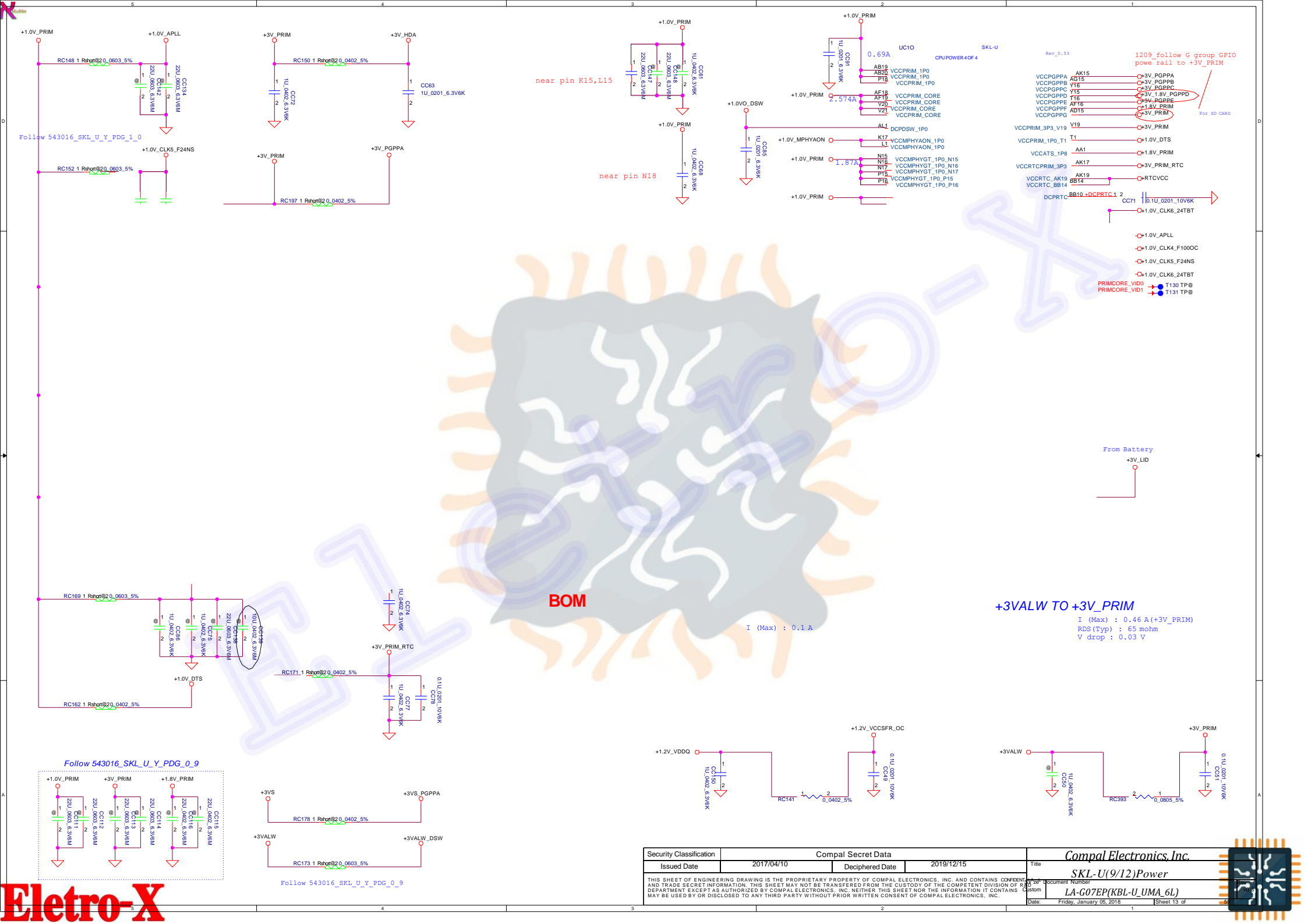


CC47 Follow 543016\_SKL\_U\_Y\_PDG\_0\_9



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Follow 543016\_SKL\_U\_Y\_PDG\_1\_0

near pin K15,L15

near pin N18

BOM

I (Max) : 0.1 A

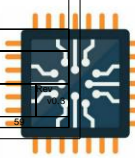
+3VALW TO +3V\_PRIM

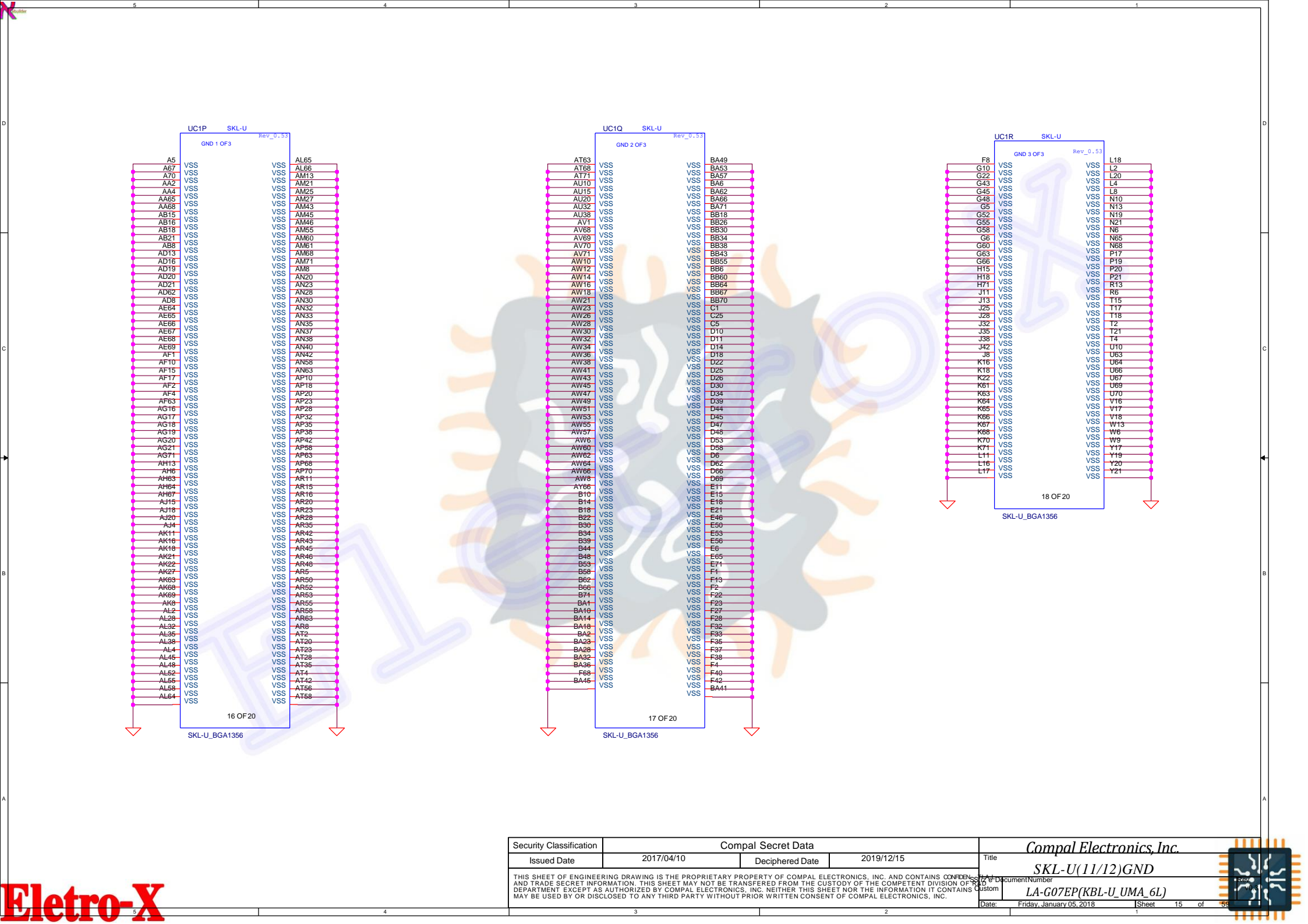
I (Max) : 0.46 A (+3V\_PRIM)  
RDS (Typ) : 65 mohm  
V drop : 0.03 V

Follow 543016\_SKL\_U\_Y\_PDG\_0\_9

Follow 543016\_SKL\_U\_Y\_PDG\_0\_9

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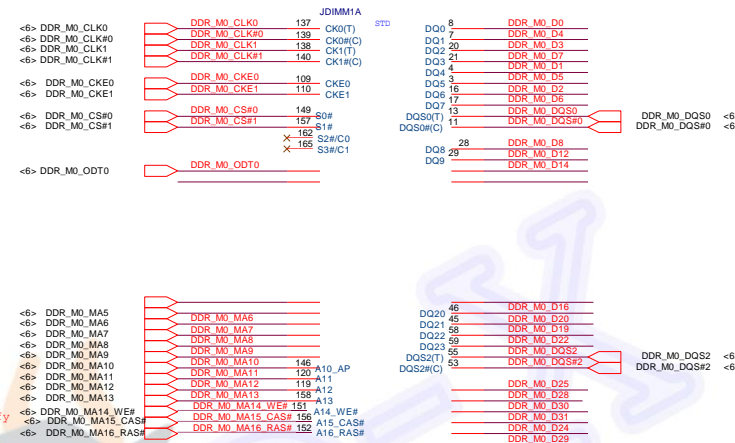


# CHANNEL-A

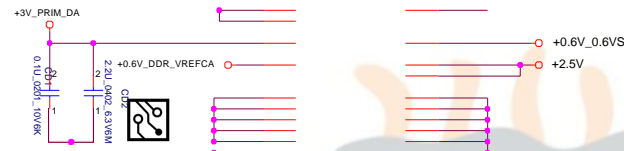
## REVERSE TYPE

### Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM

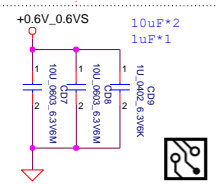
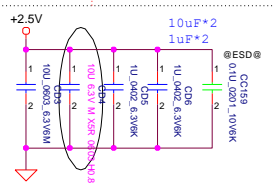


PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

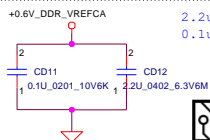


Layout Note:  
Place near JDIMM1.257,259

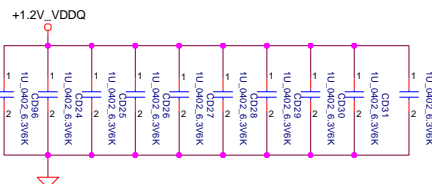
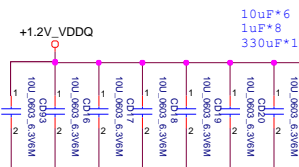
Layout Note:  
Place near JDIMM1.258



Layout Note:  
PLACE THE CAP near JDIMM1. 164



Layout Note:  
Place near JDIMM1



Part Number: LTCX0069GA0  
Part Value: S SOCKET FOX AS0A827-H2RB-7H 260P DDR4

Part Number = SF000006S00

Part Number = SF000006S00

For ECC DIMM

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

+1.2V\_VDDQ

+0.6V\_DDR\_VREFCA

+0.6V\_VREFCA

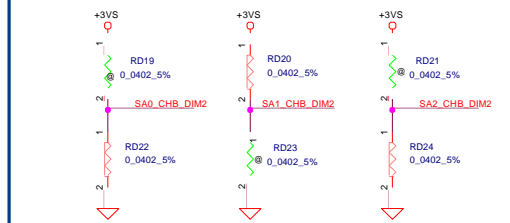


# CHANNEL-B

STD (5.2 mm)

## Interleaved Memory

TOP: JDIMM2 CONN Non-ECC DIMM

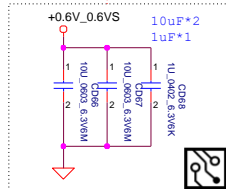
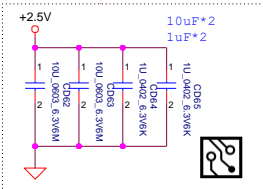


PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

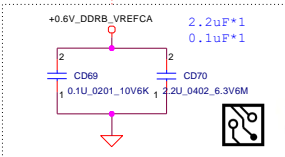
SPD ADDRESS FOR CHANNEL B :  
WRITE ADDRESS: 0XA4  
READ ADDRESS: 0XA3  
SA0 = 0; SA1 = 1; SA2 = 0.  
DDR4 POR OPERATING SPEED: 1867 MT/S  
STRETCH GOAL IS 2133 MT/S

Layout Note:  
Place near JDIMM2.257,259

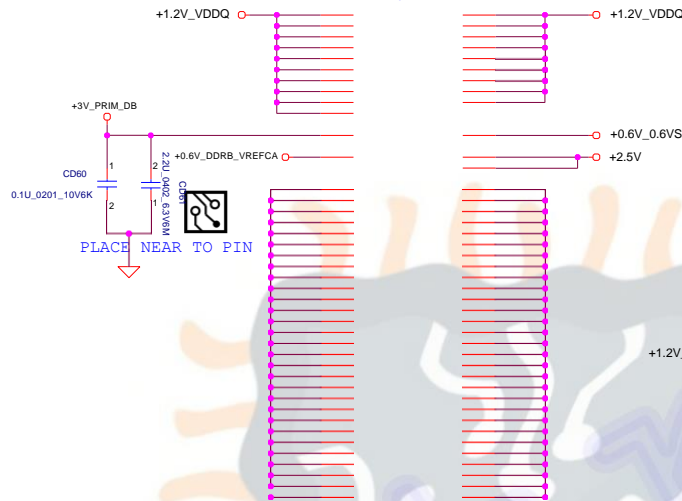
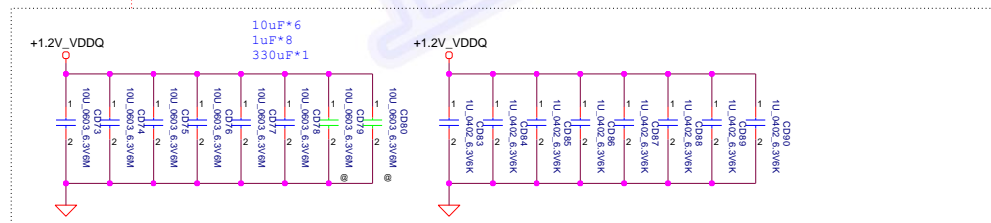
Layout Note:  
Place near JDIMM2.258



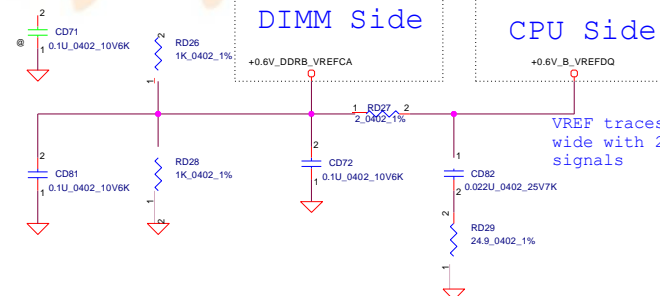
Layout Note:  
PLACE THE CAP WITHIN 200 MILS  
FROM THE JDIMM2



Layout Note:  
Place near JDIMM2



RESET#

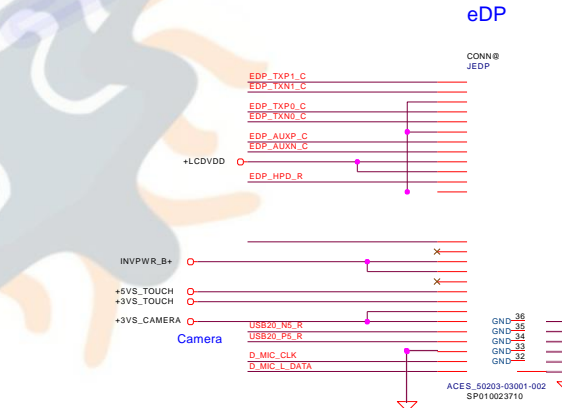
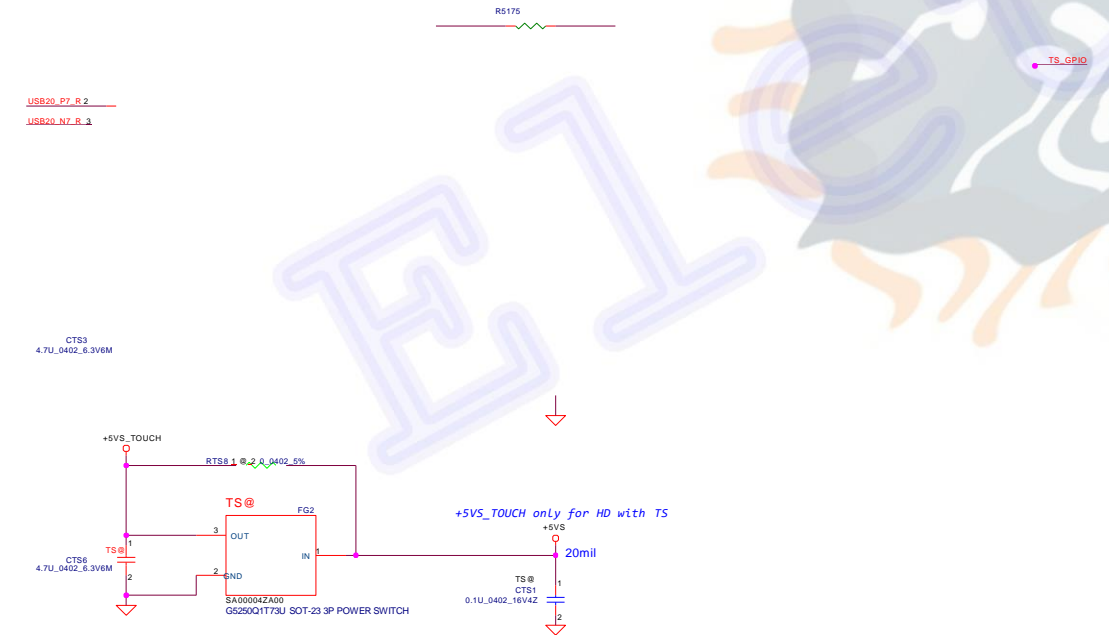


VREF traces should be at least 20 mils  
wide with 20 mils spacing to other  
signals

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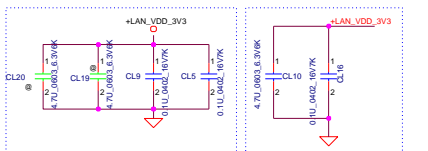
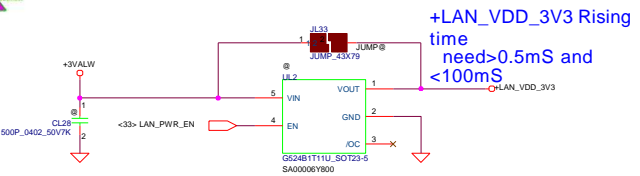


# Camera



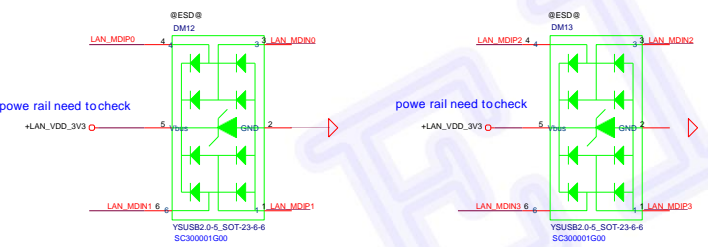
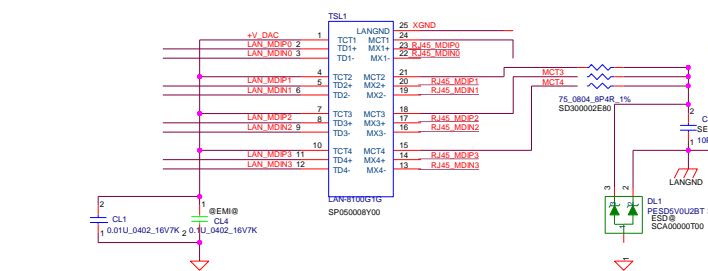
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Issued Date	2017/08/24	Deciphered Date	2018/08/24	Title	eDP CONN/Camera/TS
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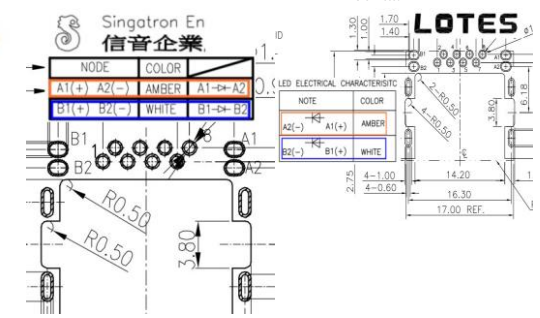
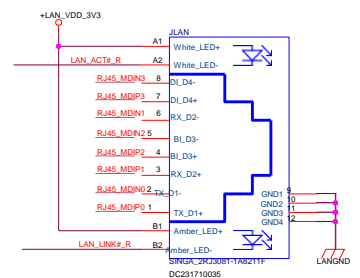
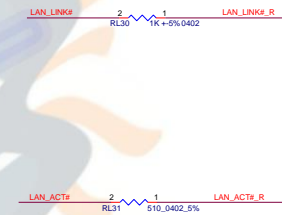


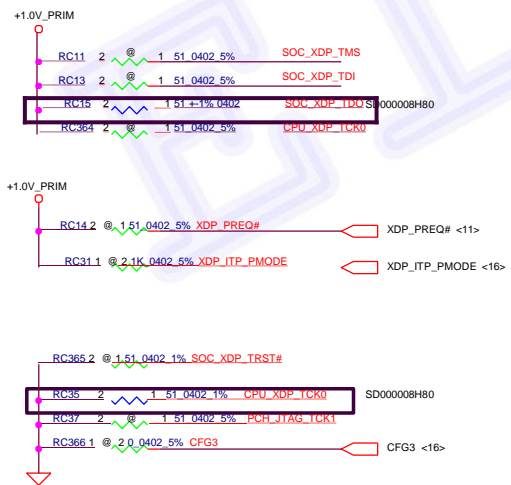
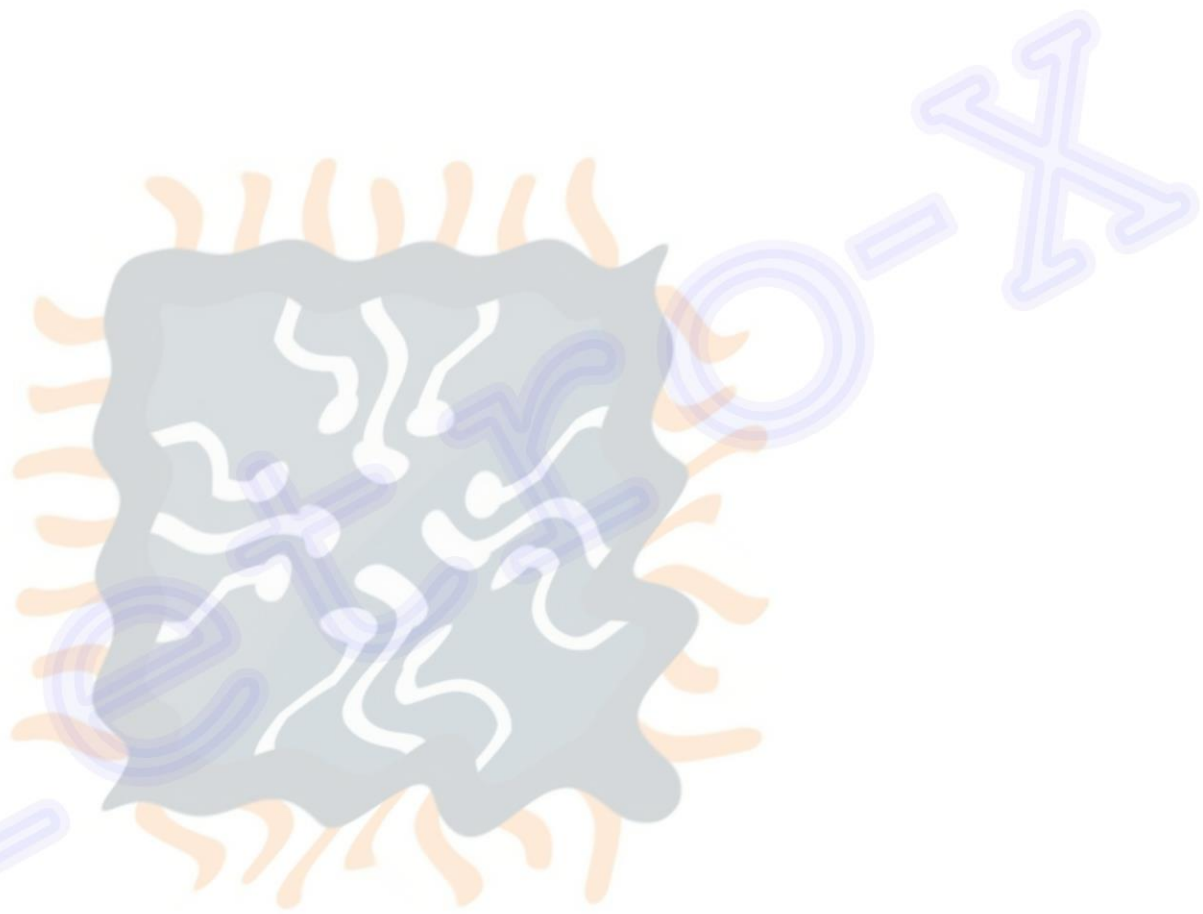
CL9, CL20 close to UL1 Pin 11  
CL5 & CL19 close to UL1: Pin 32

<B> CLK\_PCIE\_P1  
<B> CLK\_PCIE\_N1  
<11> PCIE\_CTX\_C\_DRX\_P5  
<11> PCIE\_CTX\_C\_DRX\_N5  
<11> PCIE\_CRX\_CTX\_P5  
<11> PCIE\_CRX\_CTX\_N5



# RTL8107ESH-CG/RTL8111HSH-CG Co-Lay

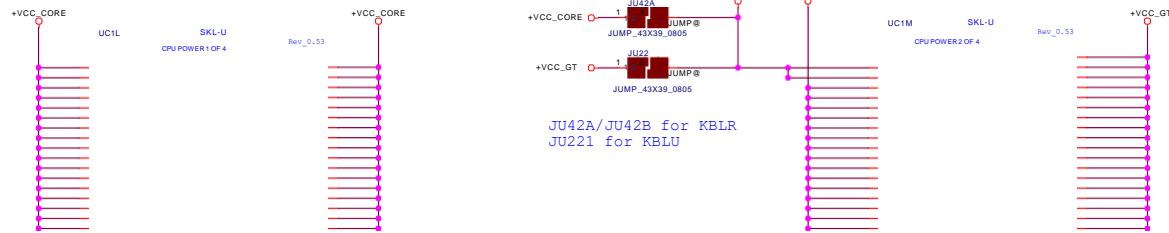




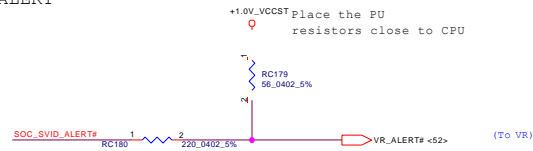
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2017/04/10	Deciphered Date	2019/12/15	Title	SKL-U(1/12)DDI.MSIC.XDP.EDP
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				Customer	
				Date	Friday, January 05, 2018
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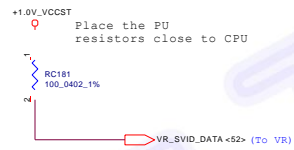




## SVID ALERT



## SVID DATA



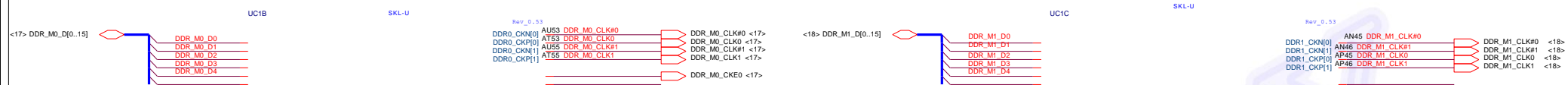
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Issued Date	2017/04/10	Deciphered Date	2019/12/15	Title	SKL-U(10/12)Power,SVID
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				Sheet	14 of 59

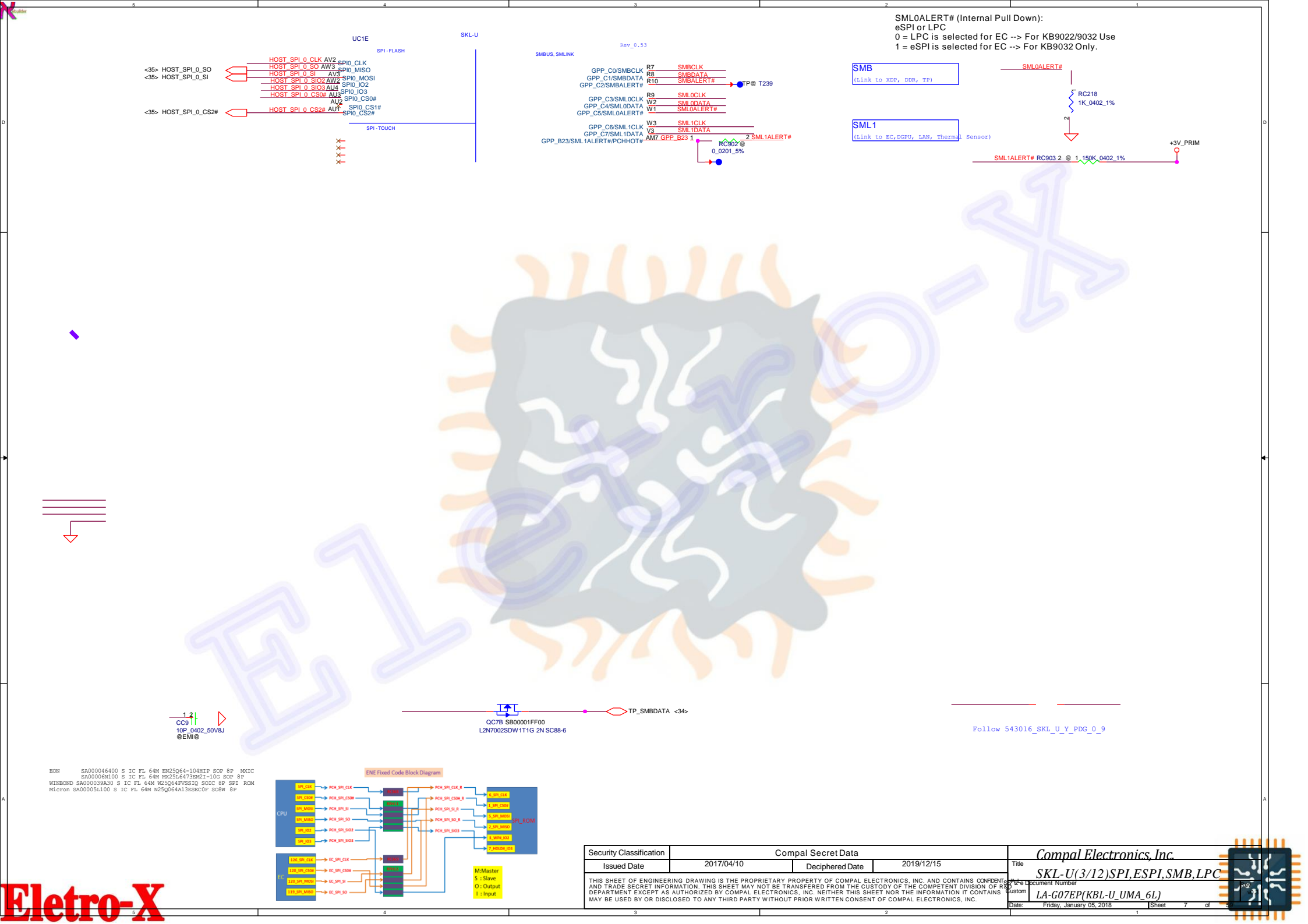


# Interleaved Memory

# Interleaved Memory

<Cocoa\_1020>  
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)





SML0ALERT# (Internal Pull Down):  
eSPI or LPC  
0 = LPC is selected for EC --> For KB9022/9032 Use  
1 = eSPI is selected for EC --> For KB9032 Only.

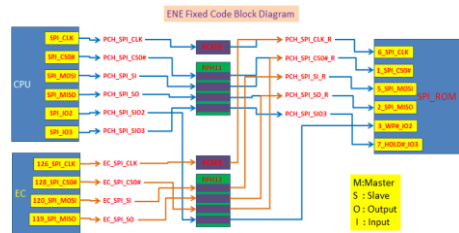
SMB  
(link to XDP, DDR, TP)

SML1  
(link to EC, GPU, LAN, Thermal Sensor)

SML1ALERT# RC903 2 @ 1 150K\_0402\_1%  
+3V\_PRIM

Follow 543016\_SKL\_U\_Y\_PDG\_0\_9

BOM SA000046400 S IC FL 64M EN25Q64-104H1P SOP 8P MXIC  
SA000008100 S IC FL 64M N25Q64-104H1P-10G SOP 8P  
WINBOND SA000039A30 S IC FL 64M N25Q64-104H1P-10G SOP 8P  
Micron SA000051100 S IC FL 64M N25Q64A13SEC0P SO8M 8P



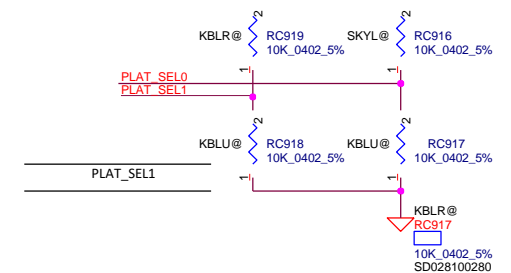
Security Classification	Compal Secret Data	
Issued Date	2017/04/10	Deciphered Date
		2019/12/15
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Title		Compal Electronics, Inc.	
SKL-U(3/12)SPI,ESPI,SMB,LPC		Document Number	
LA-G07EP(KBL-U_UMA_6L)		Custom	
Date: Friday, January 05, 2018		Sheet 7 of 8	

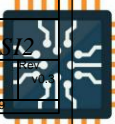
CC183  22P 50V J NPO 0402

SKL\_ULT

Rev\_0.53



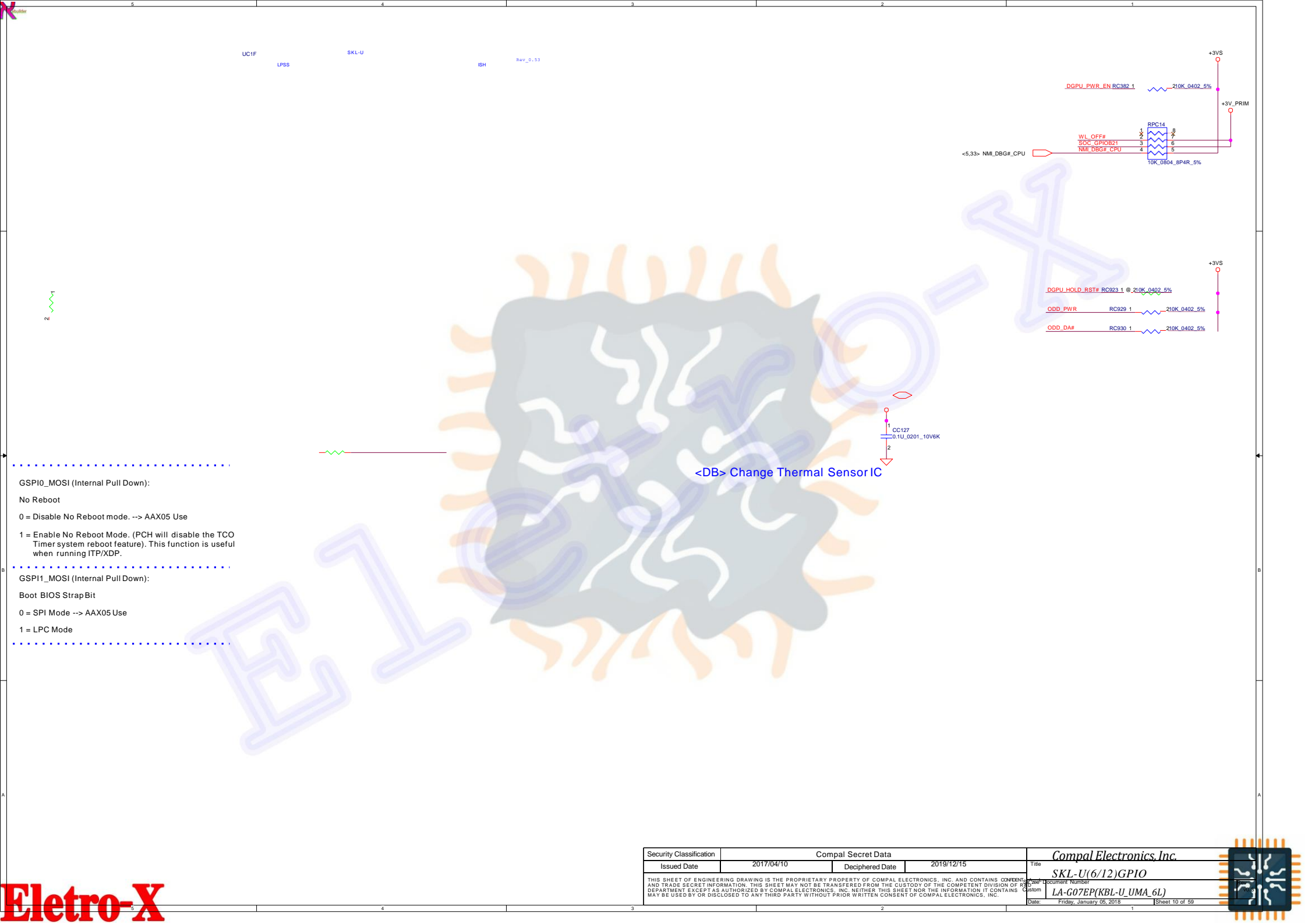
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2017/04/10	Deciphered Date	2019/12/15	Title	SKL-U(4/12)HDA,EMMC,SDIO,C	
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				Date:	Friday, January 05, 2018	
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# Eleto-X







GSPI0\_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

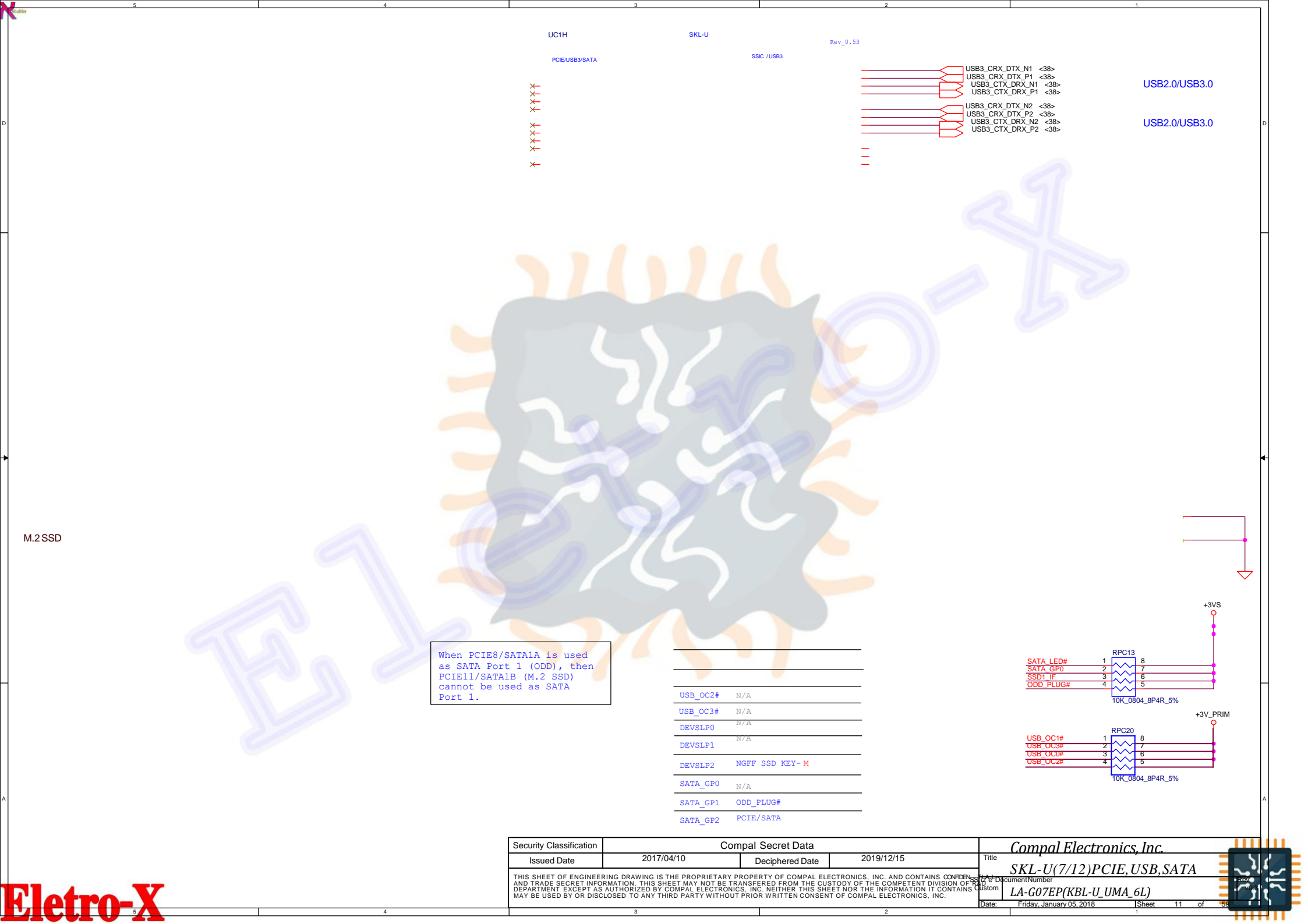
GSPI1\_MOSI (Internal Pull Down):

Boot BIOS StrapBit

0 = SPI Mode --> AAX05 Use

1 = LPC Mode

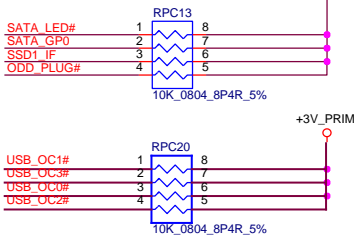
Security Classification	Compal Secret Data			Title	
Issued Date	2017/04/10	Deciphered Date	2019/12/15	Compal Electronics, Inc.	
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				Custom	LA-G07EP(KBL-U_UMA_6L)
				Date:	Friday, January 05, 2018
				Sheet 10 of 59	



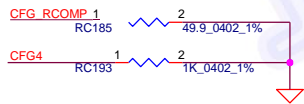
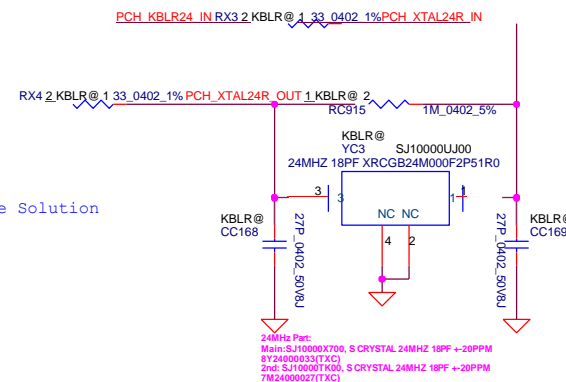
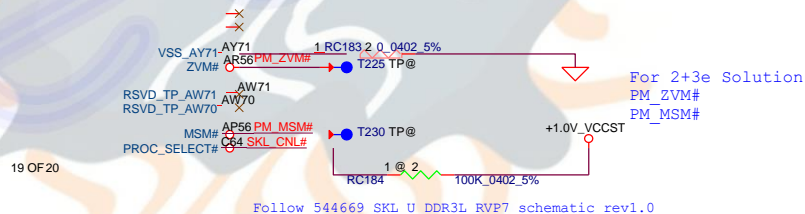
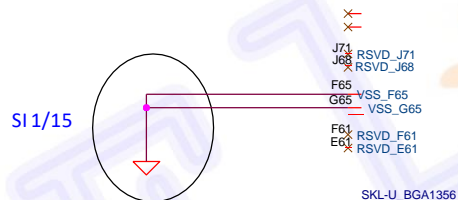
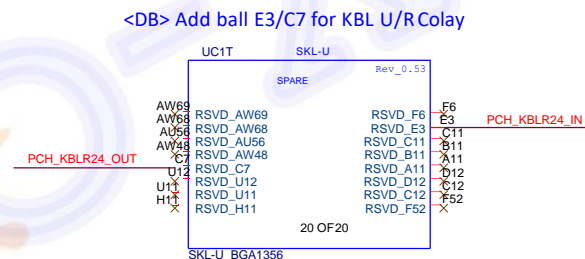
M.2 SSD

When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

USB_OC2#	N/A
USB_OC3#	N/A
DEVSLP0	N/A
DEVSLP1	N/A
DEVSLP2	NGFF SSD KEY- M
SATA__GP0	N/A
SATA__GP1	ODD_PLUG#
SATA__GP2	PCIE/SATA



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				Date	Friday, January 05, 2018
				Sheet	11 of 11



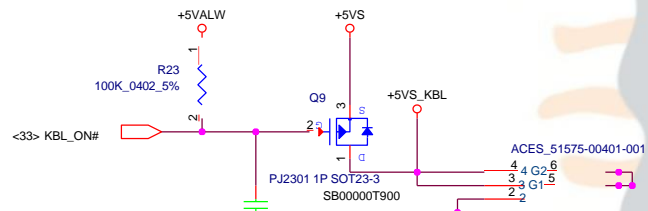
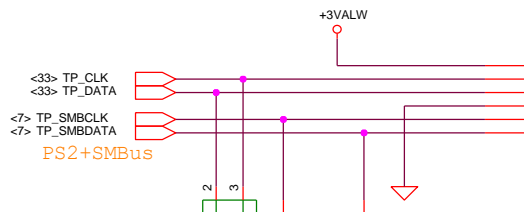
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification		Compal Secret Data		Title	
Issued Date	2017/04/10	Deciphered Date	2019/12/15	Title	SKL-U(12/12)RSVD
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				Date	Friday, January 05, 2018
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## TP Button BD Connector



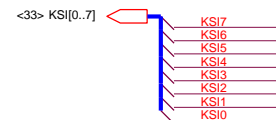
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<12,37,38,39,40,48,49,52,53> +5VALW

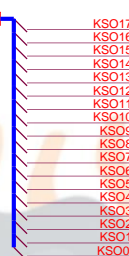
← +3VALW

← +5VALW

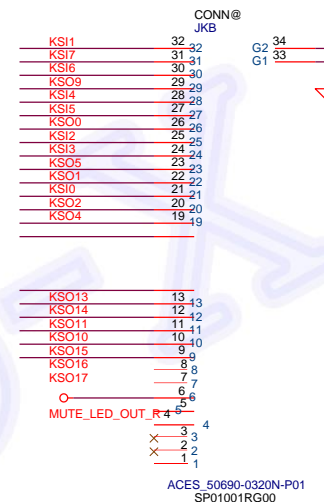
## Keyboard conn



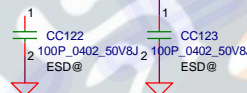
<33> KSO[0..17]



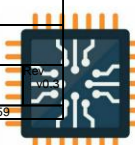
	JKB1	KB Spec
Pin1	KSI1	KSI1
Pin32	5V	5V



ESD@ C193 2 1 100P\_0402\_50V8J



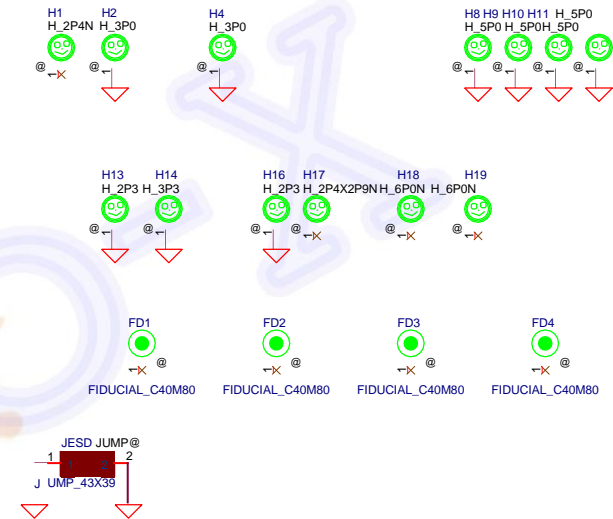
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Issued Date	2017/08/24	Deciphered Date	2018/08/24	Title
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Document Number				LA-G07EP(KBL-U_UMA_6L)
Date:				Friday, January 05, 2018
Sheet				34 of 59



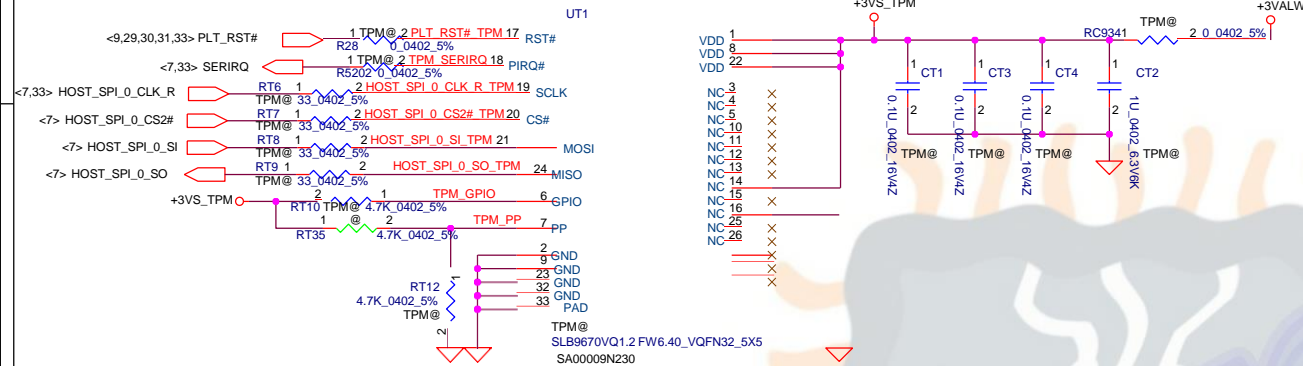
+3VALW<7,13,29,30,33,34,40,48,49,50,51>

## Screw Hole

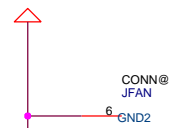
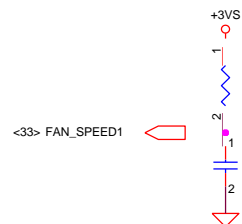
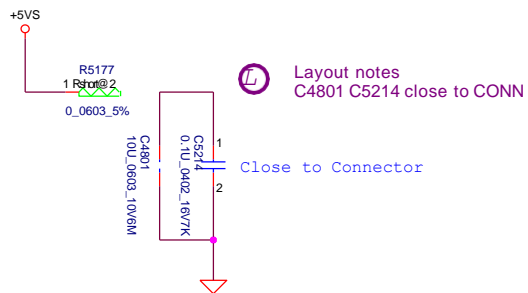
CPU



## TPM2.0



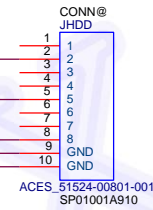
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Issued Date	2017/08/24	Deciphered Date	2018/08/24	Title	TPM/Screw
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				Date	Friday, January 05, 2018
				Sheet	35 of 35



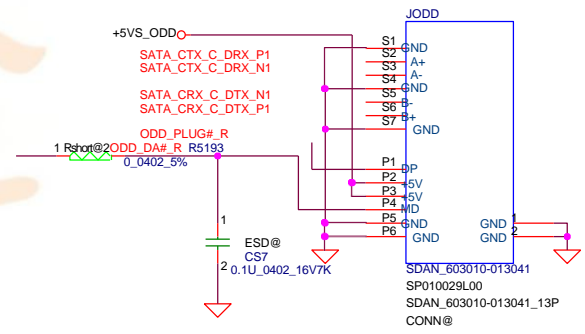
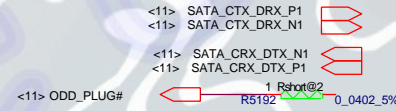
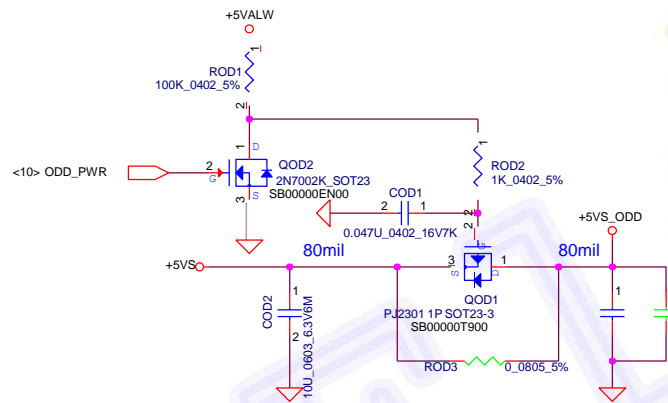
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								FAN	
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						LA-G07EP(KBL-U_UMA_6L)			
						Date			
						Friday, January 05, 2018			
						Sheet 36 of 36			

# 2.5" SATA HDD

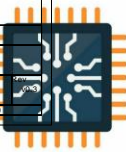
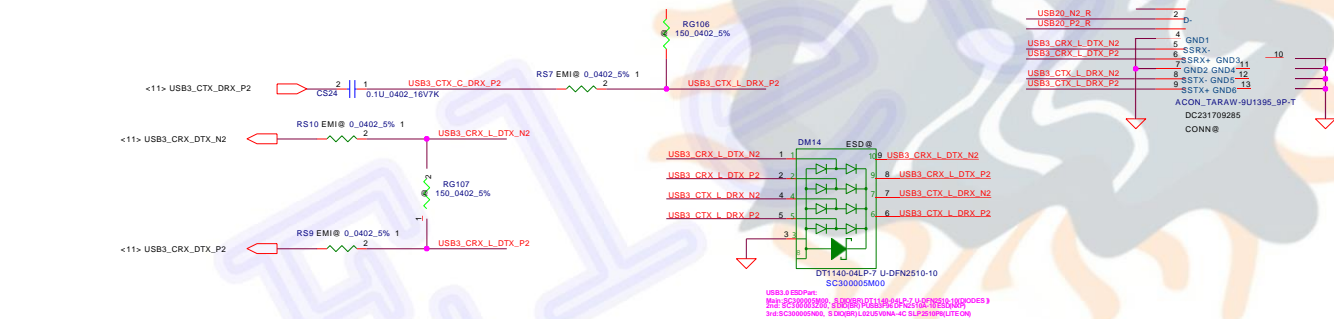
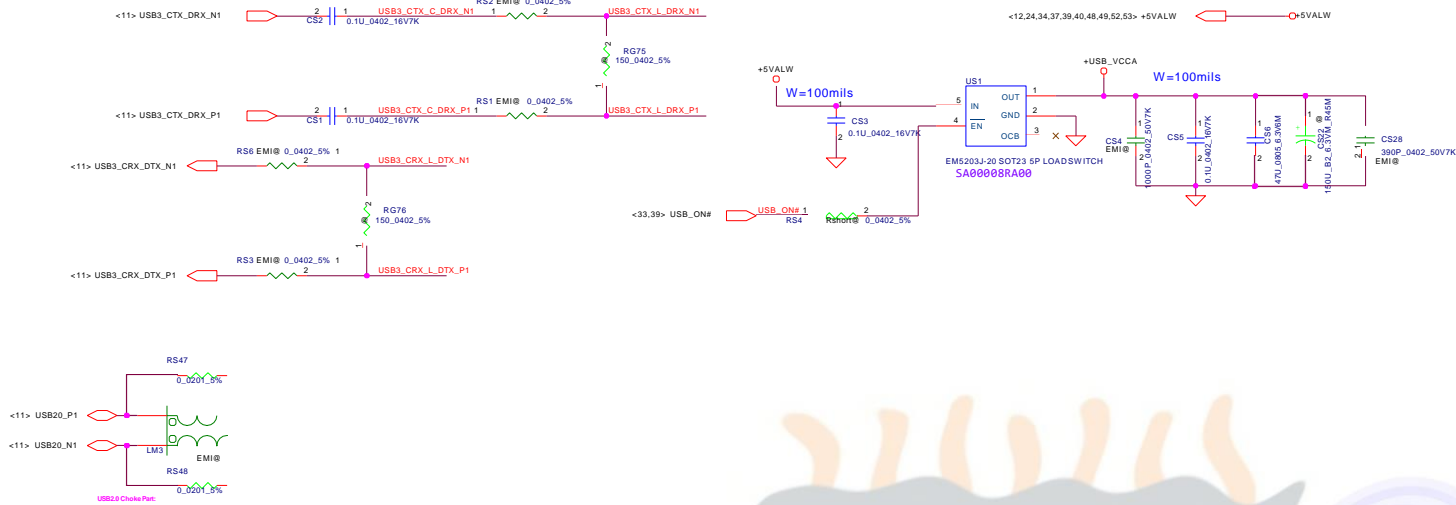
<PV> change short pad

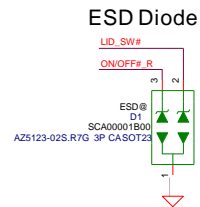
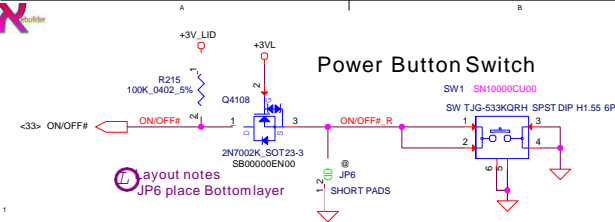


# SATA ODD

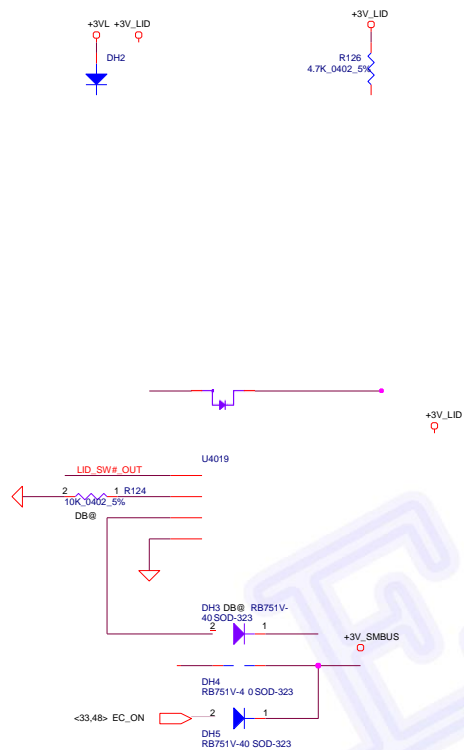






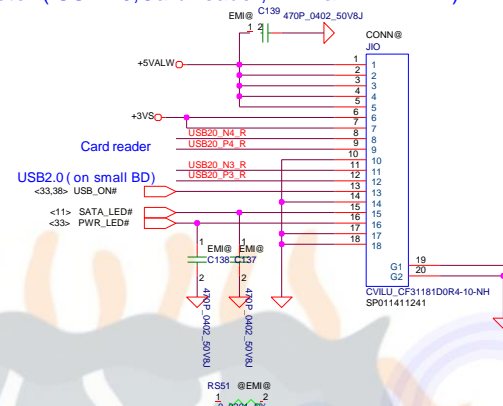


### Lid Switch (Hall Effect Sensor)



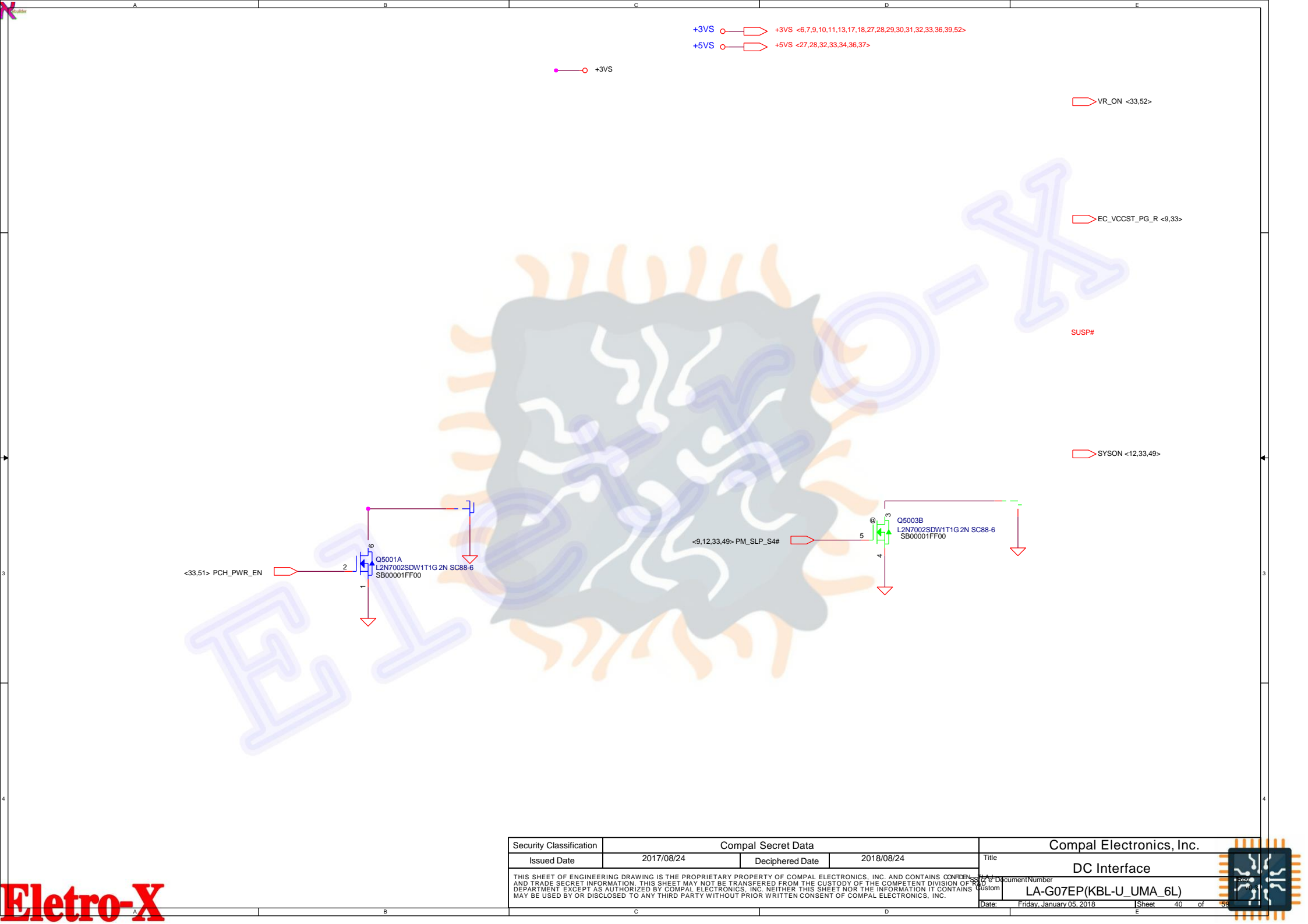
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<12,24,34,37,38,40,48,49,52,53> +5VALW  
<6,7,9,10,11,13,17,18,19,22,23,24,27,28,29,30,31,32,33,36,40,52,55> +3VS  
<7,13,29,30,33,34,35,40,48,49,50,51,55> +3VALW

### IO BD Connector ( USB2.0,Card reader,HDD & PWR LED )



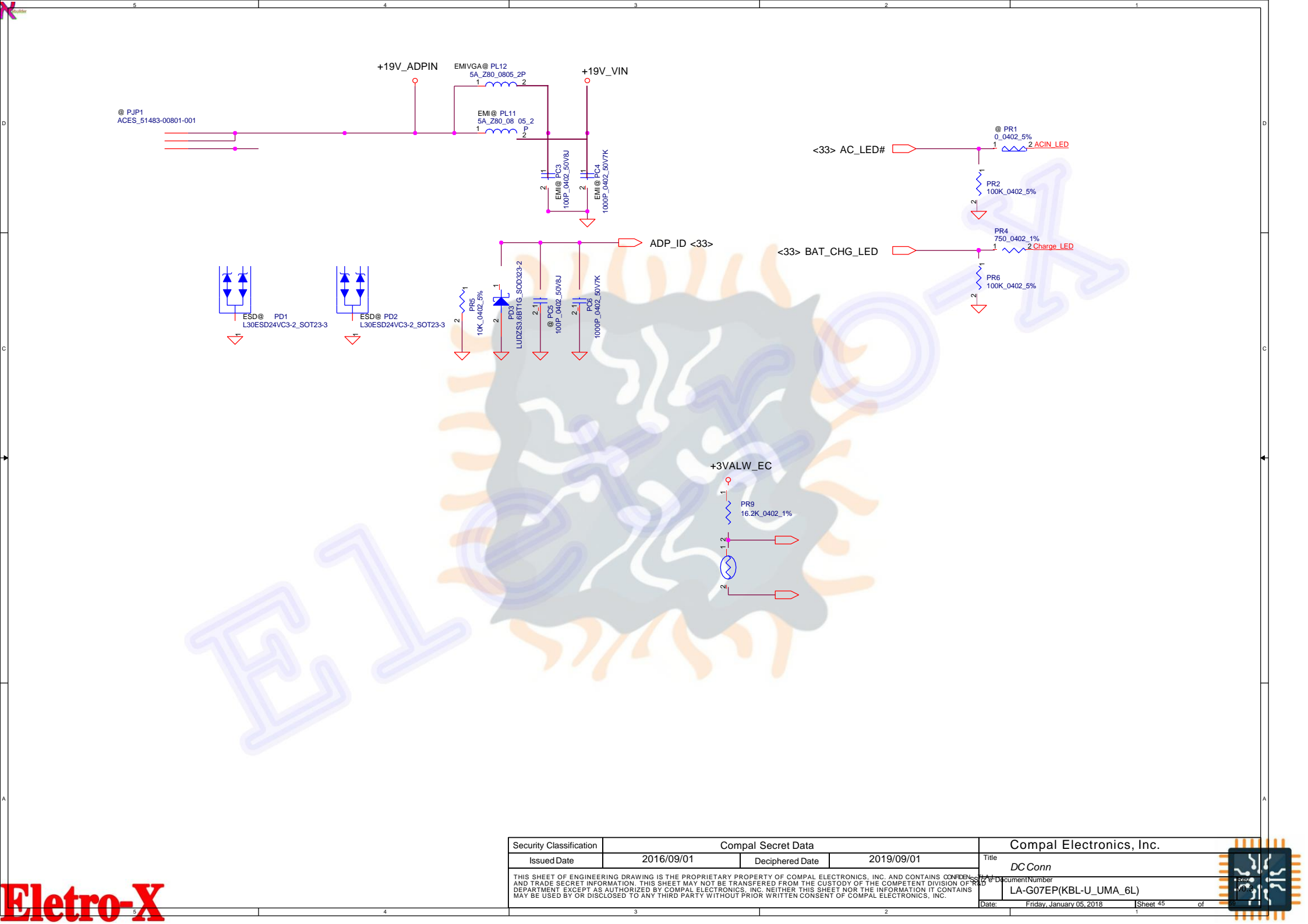
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Issued Date	2017/08/24	Deciphered Date	2018/08/24	Title	IO CON
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				Date	Tuesday, January 09, 2018
				Rev	v0.3
				Sheet	39 of 59



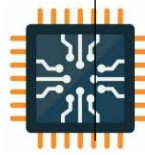
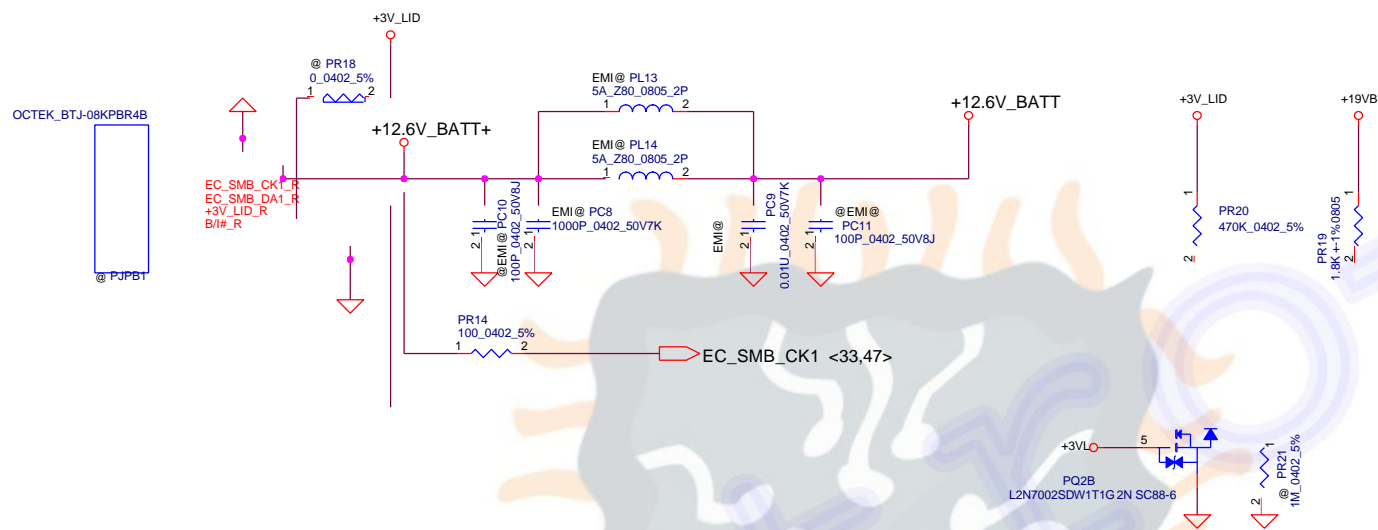


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				Date	Friday, January 05, 2018
				Sheet	40 of 50

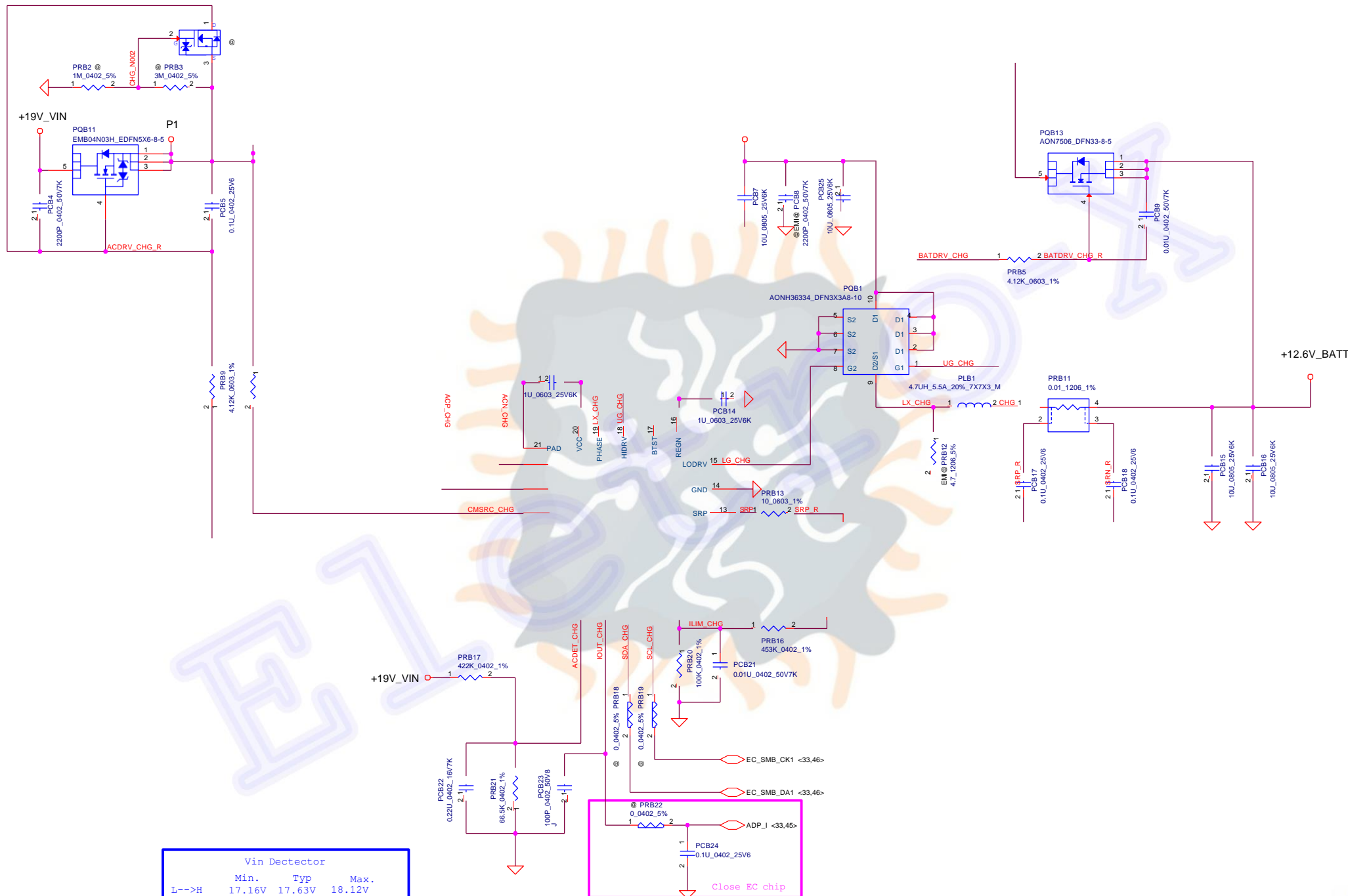






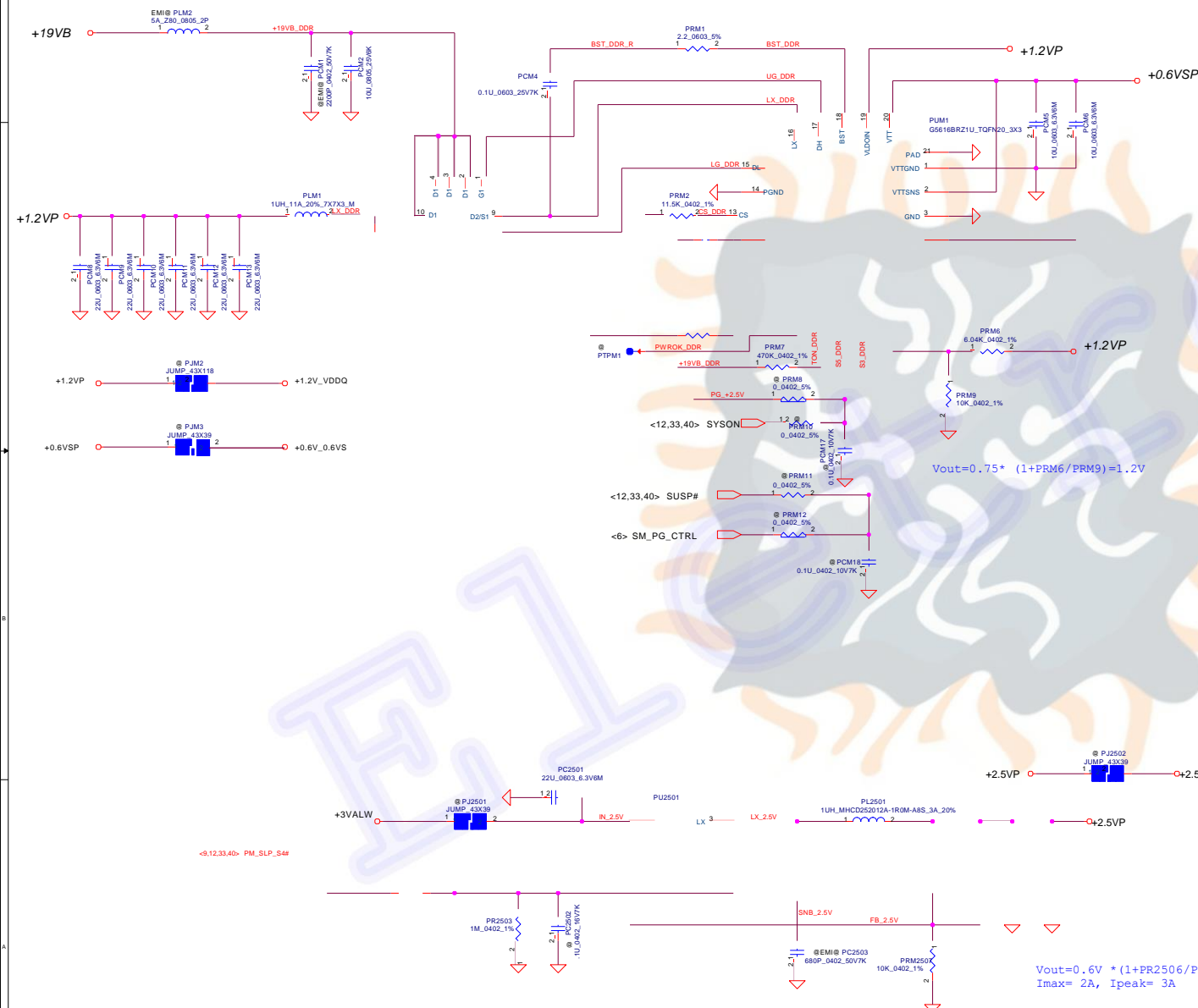


# Protection for reverse input

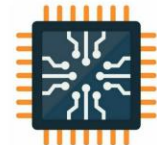


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				Date:	Friday, January 05, 2018
				Sheet	47 of 59





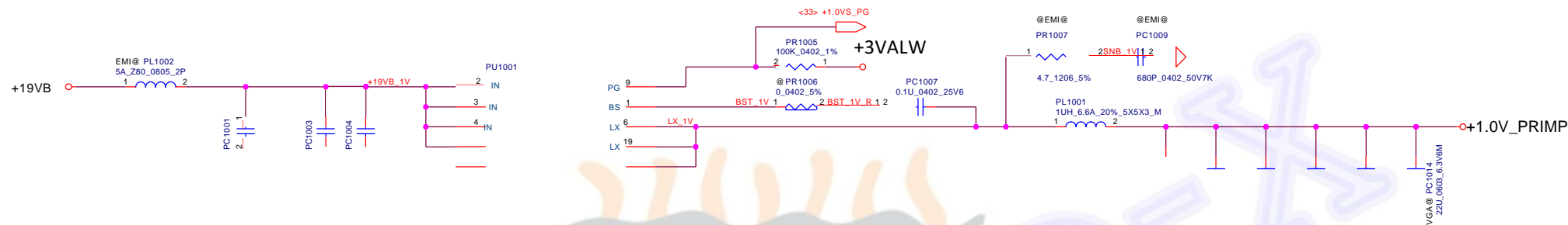
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Issued Date	2016/09/01	Deciphered Date	2019/09/01	Title	1.2VP/0.6VSP/2.5V
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				Date	Friday, January 05, 2018
				Sheet	49 of 69



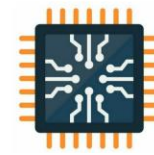
<51> +1.8V\_PG

N :H>0.8V ; L<0.4V  
N pin don't floating  
F have pull down resistor at HW side,  
lease delete PR601.

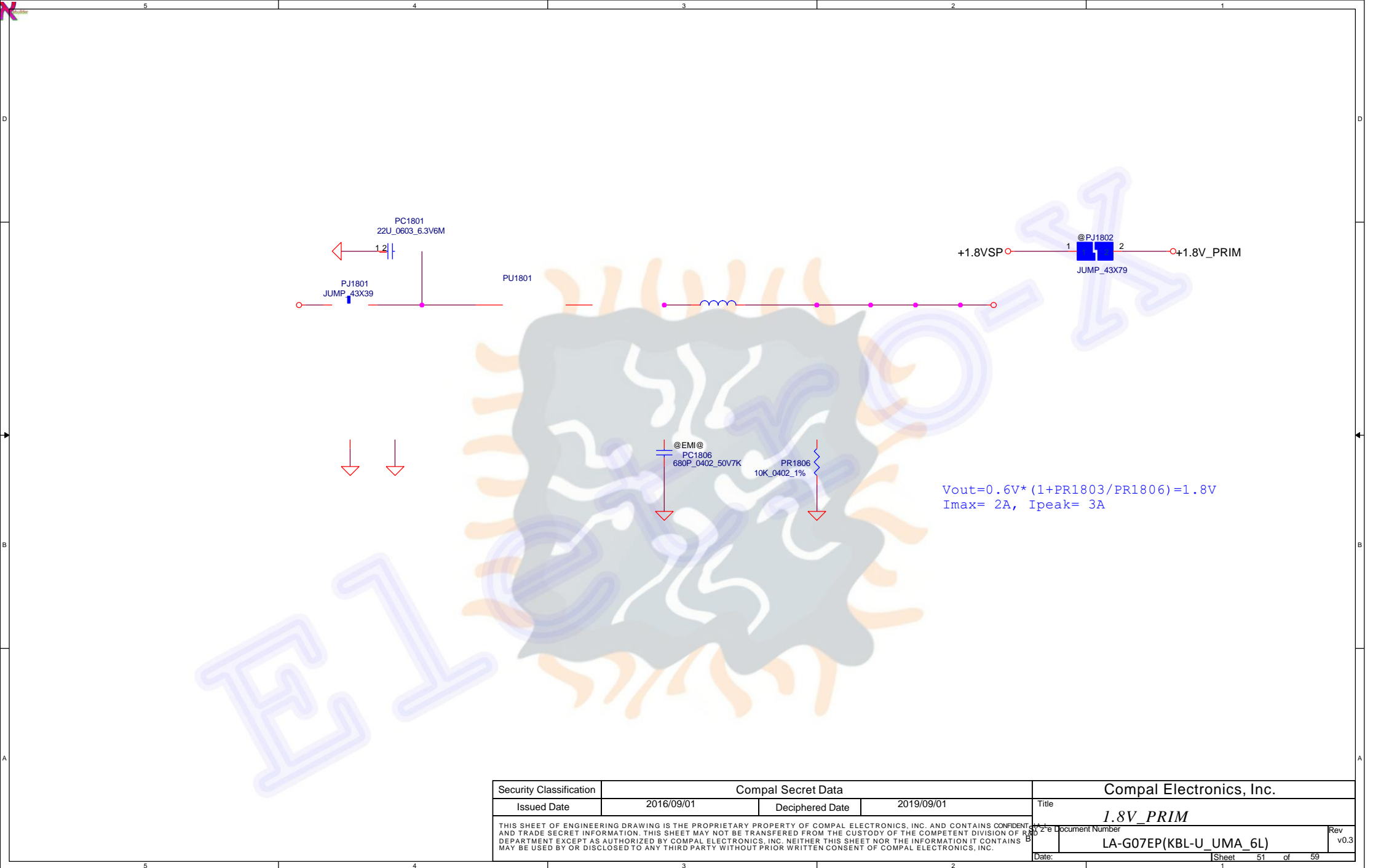
The current limit is set to 6A, 9A or 12A when this pin  
is pull low, floating or pull high.



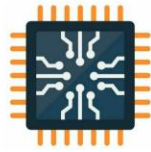
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Issued Date		2016/09/01		Deciphered Date		2019/09/01		Title	
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						Custom		v0.3	
Date:		Fri Jan 05 2018		Sheet		50		of 59	

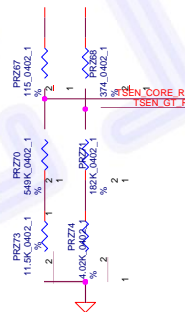







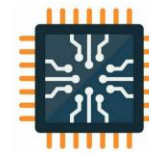
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Issued Date	2016/09/01	Deciphered Date	2019/09/01	Title	1.8V_PRIM
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U22	N/A
U42	





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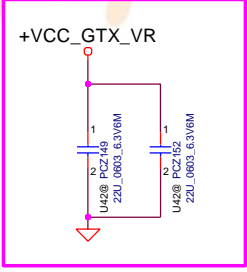
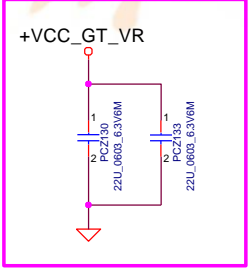
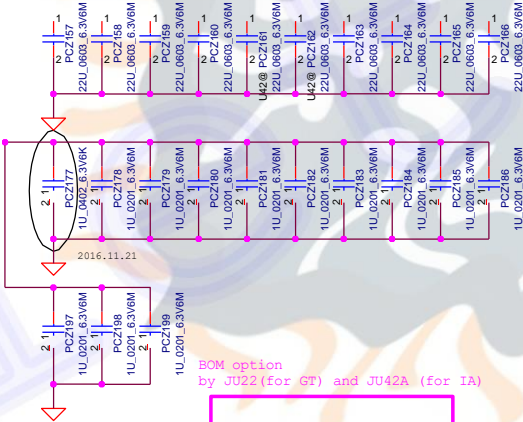
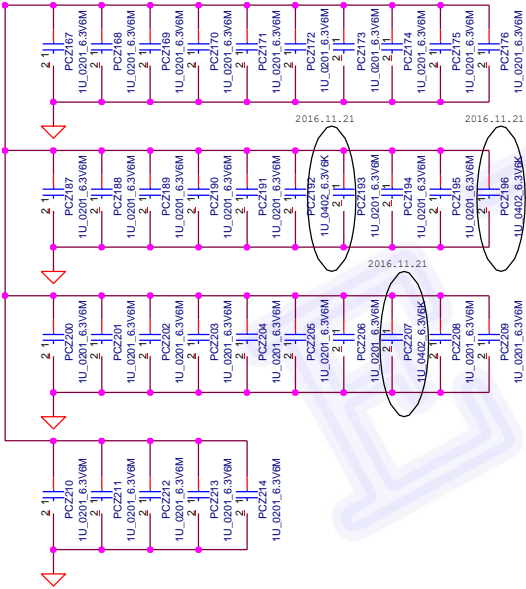
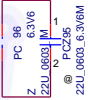
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VCC\_GT :  
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390uF\*1  
22uF\*33  
1uF\*13

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